Type	Catalog Number	Package
SDA 2006	Q67100-Q264	DIP-18

General Features

- Electrically programmable non-volatile memory fabricated in n-channel floating-gate technology
- Memory capacity: 512-bits (32x 16-bit words)
- Serial address, chip-select, and command input by 8 or 12-bit control words (length selectable by external connection).
- Erase and write duration set by external control
- Signal outputs are open-drain; active signal inputs and outputs invertible via external wiring
- Reprogrammable over 10^4 times
- Unlimited read without data loss
- Data retention of at least10 years

Absolute Maximum Ratings

Supply voltage	$U_{DD\ 2\text{-}1}$	22	V
Supply voltage	$U_{PI\ 18\text{-}1}$	22	V
Supply voltage	$U_{PH\ 3\text{-}1}$	41	V
Input voltage	$U_{I\text{-}17}$	16	V
Total power disspiation	P_{tot}	400	mW
Thermal resistance (junction to air)	$R_{th\ SU}$	90	K/W
Storage temperature	T_S	-40 to 125	°C

Typical Operating Ratings (U_{SS} = 0V)

Supply voltage	$U_{DD\ 2\text{-}1}$	11-16	V
Operating temperature	T_U	0 to 70	°C

Translated from German by Matthew D'Asaro and David Jenicek

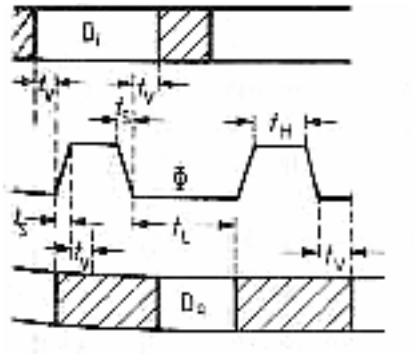
Statistical characteristics (U_{SS} = 0 V)

		min	typ	max	
Supply current	$I_{DD\,2}$		10	20	mA
Substrate bias	$-U_{BB\,1}$	4		6	V
Substrate current					
(medium current)	$-I_{BB\,1\,m}$*)		0.5	2	mA
(pulsed max current)	$-I_{BB\,1\,s}$*)			10	mA
Programming voltage	$U_{PH\,3}$*)		33	35	V
Programming current, low current	$I_{PH\,3}$		0.1		mA
Programming current, medium current	$I_{PH\,3\,m}$		2	5	mA
Programming current, pulsed max current	$I_{PH\,3\,s}$		5	10	mA
Write voltage	$U_{PH\,18}$*)		15	16	V
Write current, low current	$I_{PI\,18}$		0.1		mA
Write current, medium current	$I_{PI\,18\,m}$		5	20	mA
Write current, pulsed max current	$I_{PI\,1s\,s}$		15	20	mA
Inputs					
D_i	$U_{L\,8,12,16}$	0		0.5	V
$\Phi / \overline{\Phi}$	$U_{H\,8,12,16}$	4		V_{DD}	V
REC/$\overline{\text{REC}}$	$I_{H\,8,12,16}$			10	µA
($U_H = U_{DD}$)					
STWL					
($-I_L$ = 100µA, Pull-up-Resistors)	$U_{L\,4,15,9,11,10}$	0		0.5	V
INV	$U_{H\,4,15,9,11,10}$	4		V_{DD}	V
CS_3	$I_{H\,4,15,9,11,10}$			10	µA
CS_1, CS_2					
(Only with 12-bit word, U_H=U_{DD})	$I_{H\,4,15,9,11,10}$			10	µA
(U_L = 0V; $U_H = V_{DD}$)	$I_{L\,4,15,9,11,10}$			300	µA
$\overline{\text{RES}}$	$U_{L\,6}$	0		0.5	V
	$U_{H\,6}$	4		V_{DD}	V
(U_L = 0V)	$-I_L$			200	µA
($U_H = V_{DD}$)	I_H			200	µA
Outputs					
$D_q/\overline{D_q}, \overline{L}/L$	$U_{L\,14,13}$			0.5	V
(I_L = 1 mA; Open Drain Output)					
($U_H = V_{DD}$)	$I_{L\,14,13}$			10	µA

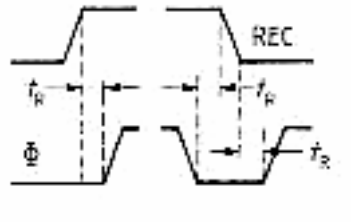
*) required during programming only

Dynamic characteristics		min	typ	max	
Bus					
Φ – Clock	t_H	5			µs
INV low	t_L	10			µs
Φ – Clock	t_H	10			µs
INV high	t_L	5			µs
	t_V	5			µs
	t_S			2	µs
Settling Time	t_R	5			µs
INV high or low					
Programming Time (U_{PH} = 33V, U_{PI} = 15V)	t_{prog}		0.1	1	s
Programming Frequency	f_{prog}			1	Hz

INV Low



Settling Time



Functional Description

Data Transfer

The SDA 2006 uses a 5-line serial bus for communicating data and commands. This bus consists of the following lines:

Data Input D_i

Data Output $D_q/\overline{D_q}$

Receiving Data $REC/\overline{REC}$ (receive data)

Clock Input $\Phi/\overline{\Phi}$

Programming signal $\overline{L}/L$ (load)

The active state (low or high) of each of these lines is set with the INV input to facilitate different application circuits.

Connection	State		Notes
INV	low (U_{SS})	high (U_{DD})	
$D_q/\overline{D_q}$	$D_i = D_q$	$D_i = \overline{D_q}$	
$REC/\overline{REC}$	high	low	During data input
$\Phi/\overline{\Phi}$	high	low	Active clock phase
$\overline{L}/L$	low	high	While programming

Chip Commands

Commands are sent to the chip via the data input, D_i. Commands are in the form of a control word whose length is set by the STWL input.

STWL connection	low	high (V_{DD} or high impedance)
Control word length	8-Bit	12-Bit

The control words encode the address of the data word to be read or modified, the chip address, and the command. They have the following format. (A0, the LSB, is sent first)

8-Bit Control Word	$A_0A_1A_2A_3A_4B_1B_2C_3$
12-Bit Control Word	$A_0A_1A_2A_3B_0B_1B_2B_3A_4C_1C_2C_3$

where A_0 ……. A_4 are address bits
B_0 ……. B_3 are command bits
C_1 ……. C_3 are chip select bits

Command Codes:

12-bit Command Word				
B_0	B_1	B_2	B_3	Command
low	high	high	high	Read out, D_9 as LSB
low	low	high	high	Read out, D_1 as LSB
low	low	low	high	Program
	8-bit Command Word			

Chip select:

Memory contents are decoded only when the chip select bits agrees with the chip select inputs and a read out command has been sent.

Chip Select - Pin		Chip Select - Bit	
	CS_1	$\leftrightarrow$ C_1	
	CS_2	$\leftrightarrow$ C_2	12-Bit Control Word
8-Bit Control Word	CS_3	$\leftrightarrow$ C_3	

CS_1 and CS_2 are inactive with 8-bit control word.

Reading (Fig. 1a and b)

Before reading, the 8- or 12-bit control word must be clocked in at the data-input D_i. 8 (or 12) clock pulses are required on the $\Phi / \overline{\Phi}$ pin to enter the control word. While entering the control word the REC/$\overline{\text{REC}}$ pin needs to be held in the active state. (Note that REC is active high when the INV pin is low and active low when the INV pin is high).

At the falling edge of the REC/$\overline{\text{REC}}$ pin, the command word is decoded and compared to the chip select pins. If they agree the data output $D_q/\overline{D_q}$ becomes low-impedance.

The read-out process is started with an additional clock pulse S. A new bit of data is output on each subsequent falling edge of the clock. The LSB is available on the data output on the first of these pulses. The control word can identify either the first bit D1 or D9 as the LSB during the read-out. The read-out process can be canceled after any number of shift impulses. Every saved 16-bit word is divided into two 8-bit words and can be read out as thus.

Programming (Fig. 2a and b)

Before programming, the 16-bit data word (D1 as LSB) and the 8/12-bit control word must be clocked in on data input D_i with REC/$\overline{\text{REC}}$ active. Upon the rear edge of the REC/REC signal, the programming command is decoded. However, the re-programming process begins only after the rear edge of an additional clock pulse. When the programming process begins the $\overline{\text{L}}$/L signal is activated.

The programming duration T_{Prog} is set by internal control. Regardless of the external control voltages U_{PH} and U_{PI}, the erase and write processes do not end until the entire memory has reached the desired state. While programming no external signals should be applied to the chip because the inputs REC/$\overline{\text{REC}}$, $\Phi / \overline{\Phi}$, and D_i are inactive. The process can only be prematurely interrupted with a low on the $\overline{\text{RES}}$ pin.

Reset function

A low voltage on input $\overline{\text{RES}}$ brings the memory to its reset state. The input has an internal voltage divider which ensures the chip is not in its reset state when $V_{DD} > 11$ V.

Voltages

The SDA 2006 has four power pins, U_{PH}, U_{PI}, U_{DD}, and U_{BB}, which are all referenced to U_{SS} (ground connection). In most applications U_{DD} and U_{PI} are connected together. U_{PH} and U_{PI} are only required during programming. They can be open or at ground during read-out and when the chip is inactive. The levels of these voltages affect only the duration, not the reliability of the non-volatile storage process.

Fig. 3 shows a practical circuit of a TV tuning-memory.

Inverted levels (INV pin high or open)

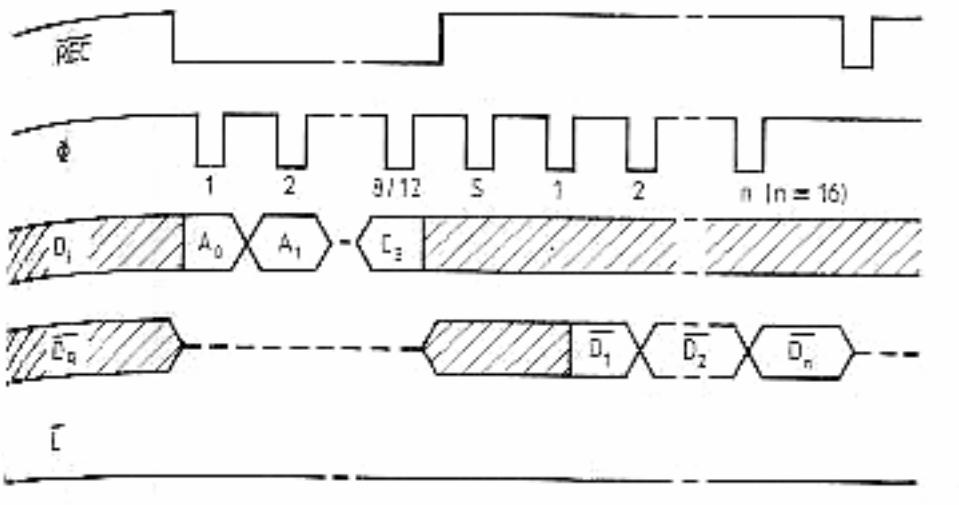


Fig. 1a

Non-Inverted levels (INV pin low)

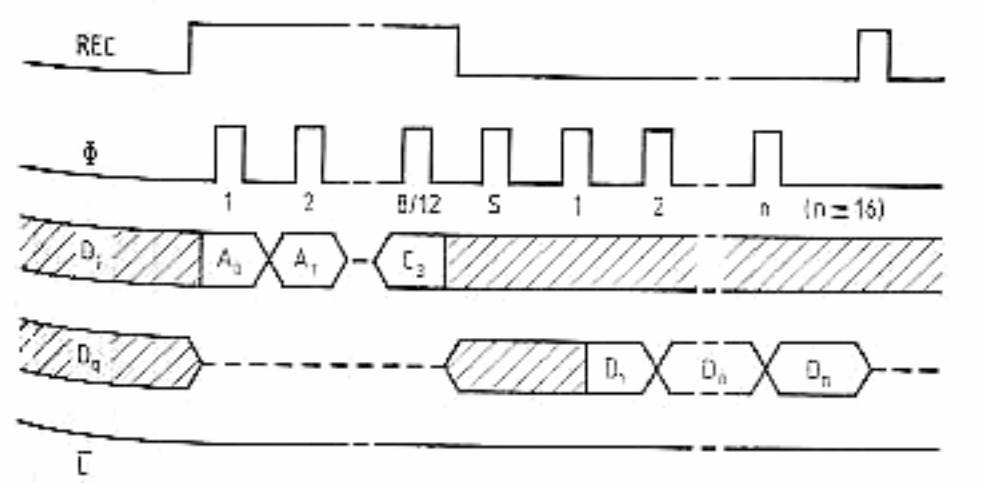


Fig. 1b

Figs. 1a and 1b show the read process (only active levels provided/specified)

Inverted levels (INV pin high or open)

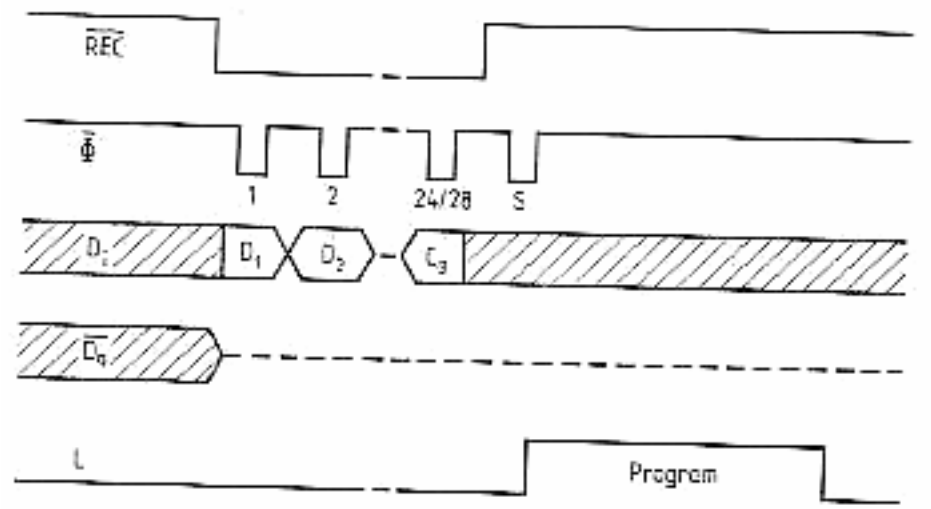
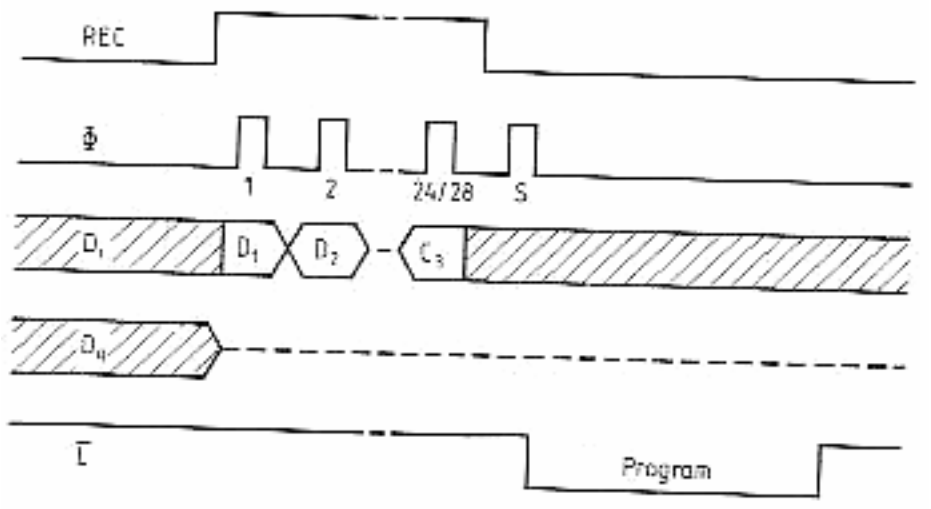


Fig. 2a

Fig. 2b



Figs. 2a and 2b show the programming process (only active levels provided/specified)

Pin Configuration

Pin Number	Symbol	Function
1	U_{BB}	Substrate bias
2	U_{DD}	Supply voltage
3	U_{PH}	Programming voltage
4	STWL	Length of control word 12 / 8 bit (input), (12-bit for high or no connection)
5		No Connection
6	$\overline{RES}$	Reset input
7		No Connection
8	D_i	Data input
9	CS_3	Chip select inputs (8 and 12-bit control word)
10	CS_2	Chip select input (12-bit control word)
11	CS_1	Chip select input (12-bit control word)
12	$\Phi / \overline{\Phi}$	Clock input *)
13	$\overline{L}/L$	Programming signal output (load) *)
14	$D_q/\overline{D_q}$	Data output *)
15	INV	Invert input signals (input)
16	$REC/\overline{REC}$	Data-input control (receive) *)
17	U_{SS}	Ground
18	U_{PI}	Write Voltage

*) First polairy for INV low. Second polarity for INV high.

Fig 3: SDA 2006 as TV tuner-memory